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Message:

Application No.	:	10/629,164	Confirmation No. 5997
Applicant	:	Pantas SUTARDJA	
Filed	:	July 28, 2003	
Title	:	DISK SYNCHRONOUS WRITE	
TC/A.U.	:	Alan FABER	
Examiner	:	2651	

PAPER ENTITLED: Response Under 37 C.F.R. § 1.111 5 pages

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PATENT **Attorney Docket No.: MP0301**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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RESPONSE UNDER 37 C.F.R. § 1.111

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Within the three-month shortened statutory period prescribed, Applicant responds as follows to the Office Action dated July 21, 2005.

Preliminarily, pursuant to MPEP § 713.04, the following contains a summary of a September 8, 2005 interview between the Examiner and the undersigned.

Applicant notes with appreciation the Examiner's time and attention during the September 8 interview. At the beginning of the interview, the undersigned noted, and the Examiner agreed, that Applicant's traversal of the election of species requirement did not require an indication of unpatentability of the respective species. Rather, an indication of genericness of claims 14, 28, and 60 was sufficient.

Also during the interview, the Examiner and the undersigned discussed the prior art rejections. The Examiner had rejected claims 14-16, 28-30, and 60-62 under 35 U.S.C. § 102(b) as anticipated by USP 5,535,067 (Rooke). The Examiner also rejected claims 17 and 63 under

35 U.S.C. § 102(b) as anticipated by USP 5,706,260 (Kishi). Applicant respectfully traversed the rejections at the interview, and repeats that traversal here, as well as a request for reconsideration and allowance of the claims.

Looking at the prior art rejections, and consistent with what the undersigned discussed at the interview, Applicant notes first that independent claims 14, 28, and 60, which Applicant believes are generic, recite an apparatus (claim 14), a method (claim 28) and an apparatus (claim 60 – "means" language) for generating a variable frequency clock signal for synchronously writing data to sectors on a rotating disk in a disk storage device. The elements in claim 14 following the preamble are as follows:

a timing apparatus for determining the period of time between two adjacent sectors, wherein the period of time between two adjacent sectors relates to phase rotation;

a phase-locked loop, responsive to a reference frequency for providing an output clock signal; and

an interpolator for adjusting the output clock signal responsive to the period of time between two adjacent sectors for synchronously writing data to the rotating disk.

Applicant submits that the prior art on which the Examiner relies fails to teach or suggest the claimed timing apparatus or the claimed interpolator. Applicant also notes that the interpolator responds to the period of time between two adjacent sectors which the timing apparatus determines.

On pages 6 and 7 of the application, referring to Fig. 3 which describes one non-limiting embodiment of the invention (and is the embodiment which Applicant has elected), a clock interpolator 306 modifies a phase locked loop frequency proportional to a phase rotation control

signal 308. As the specification describes, an interpolator circuit is known in the art to have the ability to shift the phase of a clock signal by small amounts in response to an external signal. In the embodiment of Fig. 3, a sector-to-sector timing signal provides the phase rotation control signal 308 to adjust the time base generator 301 output, thereby achieving a modified frequency clock output 309.

Thus, for example, if the spacing between two consecutive sector timing marks is increased by 0.1 percent, then the period of the modified frequency clock 309 is increased by 0.1 percent. As a result, data bits written to disk occupy a substantially fixed amount of space regardless of any apparent disk speed variation.

Applicant believes it is clear that none of the prior art teaches or suggests such an interpolator circuit.

Looking at the prior art on which the Examiner has relied, Fig. 3 of Rooke shows a synchronous write clock generator with control logic 13 which the Examiner equated to either an interpolator (claim 14); something performing the function of interpolating (claim 28); or an interpolation means (claim 60). In the claims, the interpolator, the function of interpolating, and the interpolation means respond to the period of time between two adjacent sectors. That period of time relates to phase rotation, as determined by a timing apparatus (claim 14); the function of timing (claim 28); or a timing means (claim 60). Applicant also has provided a known definition of an interpolator circuit in the specification.

Nothing in Rooke says anything about determining a period of time, related to phase rotation, between two adjacent sectors. Rooke is similarly silent about apparatus that responds to such a period of time to adjust an output clock signal, nor does Rooke say anything about an

interpolator as described and claimed in the present application. Nothing in Rooke teaches or suggests that the control logic 13 performs any kind of interpolation. Therefore, Applicant submits that Rooke neither teaches or suggests the claimed invention.

In rejecting claims 17 and 63, the Examiner also relied on Kishi, viewing element 705 in Fig. 21 of Kishi as an interpolator. However, element 705 in Kishi is a variable frequency divider. It is most certainly not an interpolator, especially as described and claimed in the present application. The variable frequency divider 705 in Kishi corresponds, if anything, to an element of the disclosed embodiments of the present application that is not even recited in the independent claims: an M-divider 305 in the elected species of Fig. 3. In any event, Kishi's variable frequency divider does not have anything to do with adjusting an output clock signal in response to a period of time between two adjacent sectors, wherein the period of time relates to phase rotation.

Kishi also is every bit as silent as Rooke about any kind of time period between two adjacent sectors being related to phase rotation, nor does Kishi talk about adjusting an output clock signal in response to such a period of time.

Moreover, in the Office Action the Examiner has read two elements of claim 17 on the same element in Fig. 21 of Kishi, namely the phase comparator 703 (which the Examiner has read on the claimed timing apparatus in claim 14 from which claim 17 depends), and the phase detector which is part of the phase lock loop of claim 17. Such a reading is improper.

Pursuant to the foregoing discussion, Applicant submits that all of elected claims 14-17, 28-30, and 60-63 in the present application are patentable.